MEMORY CIRCUIT SCAN ARRANGEMENT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a full scan arrangement for testing digital circuits, in particular testing using scan chains with memory circuits.

Description of the Related Art

The testing of digital circuits using scan chains is well-known to those skilled in the art. In brief, a scan chain is a series of linked flip-flops which are arranged through areas of combinatorial logic on an integrated digital circuit. Each flip-flop receives an input from the previous flip-flop in the chain, and from the combinatorial logic through which the chain passes. At an input pin, a test pattern of logic l's and O's is input to the scan chain, and passes through the sequence of flip-flops and combinatorial logic to an output pin. The output sequence of logic l's and O's is changed from the input sequence by operation of the logic under test. The manner in which the sequence is changed is not important to determining whether the circuit is functioning correctly. The circuit can be determined to pass or fail the test by simply comparing the output sequence with the output sequence of a correctly functioning circuit.

To facilitate scanning, it is known to use software for automatic generation of the test sequences of logic l's and O's, known as test patterns, and to perform analysis. Such tools are known as Automatic Test Pattern Generation (ATPG) tools and are integral to full scan testing. A known example is Tetramax ™ of Synopsys, Inc. Whilst this tool facilitates testing, on large chips the testing task is significant. On recent graphics chips designs there can be 170 scan chains with 2,600 flip-flops each. This results in excessive vector count and/or low test coverage.

We have appreciated the difficulty in testing integrated semiconductor circuits which contain one or more memory components.

BRIEF SUMMARY OF THE INVENTION

The invention is defined in the independent claims to which reference is directed. Preferred features are set out in the dependent claims.

In a method aspect of an embodiment of the invention described, a memory within an integrated circuit to be tested is loaded with a known bit sequence prior to testing. The memory thus configured provides a known output for a given input and can be modelled by combinational logic. In effect, the memory is rendered predictable so that its terminals and the surrounding circuitry can be tested.

In an apparatus aspect of the embodiment, circuitry providing an interface for a circuit to be tested is provided, known as a "wrapper". The wrapper circuit includes a preloader which is a circuit arranged to generate and provide a known bit sequence to write to the memory within the circuit to be tested.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying figures, in which:

Figure 1 shows a scan chain within an integrated circuit;

Figure 2 shows conventional scan chain inputs and outputs;

Figure 3 shows a scan chain within an integrated circuit which includes a memory;

Figure 4 shows the overall circuit of a memory embodying the invention;

Figure 5 shows the control logic for the memory of Figure 4 including preloader circuitry;

Figure 6 shows the memory preloader part of the circuit embodying the invention; and

Figure 7 shows a memory pattern for RAM;

Figure 8 shows a data generator for the memory pattern of Figure 7;

Figure 9 shows the logic equivalent circuit for a RAM preloaded with the pattern of Figure 7;

Figure 10 shows a data generator for CAM;

Figure 11 shows the logic equivalent circuit for a preloaded CAM;

Figure 12 shows the overall view of a testing arrangement with preloaded memory.

DETAILED DESCRIPTION OF THE INVENTION

The embodiment described comprises an arrangement of scan chains and outputs for testing a digital integrated circuit, and also a digital integrated circuit including the scan chain arrangement in which a memory is configured with a known pattern prior to testing. A schematic view of a scan chain is shown in Figure 1 by way of background.

A scan chain 2 comprises a sequence of latches or flip-flops 8 arranged serially between an input pin 4 and an output pin 6. Each flip-flop 8 provides the input to the logic blocks 10 and to the next flip-flop in the chain, and also receives signals from the circuitry logic under test. The circuit logic is shown as logic blocks 10 and can be any logic on a chip, such as a graphics controller. In practice, the logic cloud will comprise millions of components as an integrated circuit chip. Similarly, there will be hundreds of scan chains, each comprising thousands of flip-flops, with an input and an output pin for each chain. The chip 1 as a whole is manufactured with the scan chains built in for testing purposes and presents the input pin 4 and output pin 6 at the chip boundary 12.

A conventional scan chain arrangement is shown in Figure 2. As shown, a series of scan chains 2 are provided which pass through a logic circuit 1 under test (with many discrete logic components, not shown) between input pin 4 and output pin 6 for input signals 14 and output signals 16. The pins are located at the chip interface boundary 12 and can be bonding pads, contact points, probe sites, testing terminals, internal circuit connection points, I/O ports, or any other structure that permits transfer of signals for input to and output from the circuits, all of which are included within the meaning of the term pin as used herein. To test the circuit 1 a series of logic bits of l's and O's is input at each input pin 4 to one of the respective scan chains 1 to N. The series of bits is known as a test pattern, and is typically provided by an Automatic Test Pattern Generator (ATPG) as

previously described. The output from each output pin will be a pattern of l's and O's produced as a result of the interaction of the test pattern with the logic of the chip 1. A known correctly functioning chip will produce a given response to a given test pattern at each output pin 6. If there is a defect within the chip, this will be shown up as a difference in one or more of the output sequences. The location of the defect can then be derived, to an extent, from the position of the difference occurring in the test output patterns, and from which scan chains show differences from the expected output. This arrangement is valuable in both determining whether the chip passes the test and, if not, the approximate location of the defect.

The known scan chain arrangement described is well-known and can use existing ATPG tools such as those of Synopsys, Inc. previously mentioned, and is easy to debug in the sense that defects in the chips tested can be located by determining the scan chain (or chains) closest to where the error occurs. However, we have appreciated problems in using this technique when testing circuits which contain one or more memory elements; as shown in Figure 3.

The scan chain arrangement of Figure 3 comprises scan chains 2 receiving input signals 14 via respective input pins 4 as before. The scan chains are within logic circuitry of a chip 1 defined by a chip boundary 12. As before, each scan chain comprises a sequence of flip flops 8 which shift a bit sequence, or test pattern, from the input pin 4 to an output pin 6. Now in addition to combinational logic components represented by logic blocks 10, a memory 20 forms part of the circuit 1.

The memory 20 has a read address port (RA) 21 and an output port (Q) 22. The memory output is determined by the selected address and the contents at that address. However, in normal operation, at any given time, the memory contents may not be known. Accordingly, when testing using ATPG, the memory's data outputs may be undefined for any selected address, and the memory may therefore behave as a blockage. This will mean that logic up to and including the address inputs may be unobservable, and logic from the data outputs onwards may be uncontrollable. To avoid this problem, a wrapper circuit

having control logic is provided to write known data patterns to the RAM 20 prior to testing the whole integrated circuit 1, as shown in figure 4.

The integrated circuit embodying the invention comprises a core 30 and a wrapper 40. The core comprises a RAM array 20, the contents of which are to be configured prior to testing, and read decoder 31, write decoder 32 and control 33 for interfacing the RAM array 20 to the wrapper 40. The wrapper 40 itself is an interface circuit to provide external connection and control of the RAM 20 to allow control prior to running test patterns. The wrapper 40 comprises various ports, and three clocked D type latches 50, 51, 52. A read address port of width 6 bits (RA) 41 provides the addresses for which the contents should be presented at RAM output (Q) 48. The read address port 41 applies the address via read decoder 31. Similarly, a write address port of width 6 bits 42 provides the address to which data should be written in RAM via a write decoder 32. The write address signal (WA) from the write address port 42 is latched through a scan flip-flops 50 under control of a RAM clock signal for write access (RAM CLK) at RAM clock port 45. Similarly, the data (4 to 64 bits) D[n:o] to be written to the address given by the write address signal is presented at a data port 44 and clocked through scan flip-flops 52. The data is then presented direct to the memory 20. The write part is therefore synchronous and advantageously the scan flip-flops allow observability of preceding logic outside the RAM. The read port, on the other hand, is asynchronous and so passes data through it in the same clock cycle, making it suitable for combinational ATPG test patterns.

It is noted at this point that no additional components are required in the read address (RA) path 41 which advantageously therefore does not affect the timing of read operations.

The memory circuit can have several different configurations, including either random access memory (RAM) or content addressable memory (CAM), and may have sizes from 8 words by 8 bits to 64 words by 128 bits, for example. They all have the same basic architecture: synchronous write, asynchronous read/and or Compare, and level sensitive test write control.

For example:

Dual Port RAM -DPR : 1 write port, 1 read port.

Triple Port RAM -TPR : 1 write port, 2 read port.

Quad Port RAM -QPR : 4 write port, 4 read port.

RAM Cam -RC : 1 write port, 1 read port, 1 compare port.

Quad Port RAM -QPC : 4 write port, 4 compare port

These are all different examples of a memory circuit which could benefit from the present invention.

The DPR model can be found in all configurations (up to 64 words x 128 Bits).

There are two variants on the basic DPR RAM:

-a) Registered read address.

-b) Word-Enabled write port.

The TPR model is found in 32 X 32.

The RC model is found 16 X 11 and 16 X 22.

The QPR model is found in 32 X 32.

The QPC model is found in 32 X 22.

TPR, DPR and QPR are RAM, whereas RC and QPC are addressable content memory. (However RC is a RAM and a CAM).

The functions of the wrapper circuit 40 to allow the memory to operate in a normal mode, or selectively to fill the memory with a predefined pattern for testing are controlled by a NOT WRITE signal at write enable port 43 (active low), a WENTST signal at test write clock port 47 and a TESTMODE signal at test mode enable port 46. These signals are applied to a control block 33 whose logic functions are shown expanded in Figure 5.

The TESTMODE signal at port 46 defines whether the memory 20 is set to test mode, and is applied to AND gate 60 along with the WENTST signal at port 47. When the TESTMODE signal is logic 'O', the output of AND gate 60 is zero so that NOR gate 62 is not blocked. The TESTMODE signal is also applied to NOR gate 66 which also receives the RAMCLK signal on port 45. The delayed output of NOR gate 66 thus follows the RAMCLK signal with the result that the write strobe input 65 effectively the delayed RAMCLK signal AND'd with an inverted version of the NOT WRITE signal. In this mode, the RAM is in normal operation and data may be written to and read from the memory. When the WENTST signal is set to logic '1', and the TESTMODE signal remains logic '0' the RAM 20 is set to preload mode. The AND gate 61 has output logic '1' which is provided to counter 68 as one counter enable signal and to AND gate 67. The counter 68 is reset to zero by RSTN and is clocked by the RAMCLK signal on port 45; and counts until the counter output reaches a predetermined value, at which point a comparator 69 produces an output signal which disables further incrementing of the counter and connects to AND gate 67. The AND gate 67 controls multiplexer 63, so that a logic '1' is presented from the multiplexer to OR gate 62 so that the write strobe is active for a given number of counts, and then reverts to inactive when the counter 68 and comparator 69 cause the AND gate 67 to switch the multiplexer 63 to the NOTWRITE signal 43 which will normally be logic '1'.

When both TESTMODE and WENTST are set to logic '1', the output 68 of NOR gate 62 is set to logic '0' and the system is in combinatorial ATPG mode with write operations inhibited. Lastly, when the WENTST signal is a clock value, the RAM is in pattern wrapping test mode. This is summarized in the following table:

TESTMODE	WENTST	Function
0	0	Normal Functional Operation
0	1	Preload Ram Array
1	1	Combinational ATPG
1	Clock	Sequential ATPG (pattern mapping)

To preload the RAM with a predefined pattern, the wrapper circuit 40 includes a preloader having pattern generation and loading logic 70 as shown in Figure 6. The preloader part of the wrapper circuit 40 comprises the ports interfaces and latches as shown and described in relation to Figure 5, however, these are not shown for simplicity. Again, it is noted that the wrapper circuit does not introduce any components in the read access (RA) path.

The preloader loading logic 70 comprises a control 94, data generator 92 and address generator 90 and three multiplexers 73, 74, 75. A write address multiplexer 73 multiplexes a write address port 42a with an output line 80 of the address generator 90 to write address port 42. Similarly, a data multiplexer 74 multiplexes the data output 81 of generator 92 with a data input port 44a to data port 44. Lastly, NOT WRITE multiplexer 75 multiplexes a NOTWRITE port 43a with logic '0'

When a reset is asserted, the counter 68 is reset and the multiplexers 73, 74,75 are switched to receive inputs from address generator 90 and data generator 92 and logic '0' on lines 80, 81,82 by multiplexer control line 76. The data generator 92 and address generator 90 are reset. When the address generator reaches the maximum address of the RAM, the output of the comparator 69 is false and the multiplexers 73, 74,75 switch back so that write access 42a, data 44a and NOTWRITE 43a connect to their respective ports 42, 44, 43. The TESTMODE signal 46 at write enable port 43 is activated when the pattern has been written to the memory. This effectively turns the RAM into a ROM having predictable combinational properties as previously described.

The choice of pattern and data generator configuration depends upon the type and size of memory used. Any pattern in the memory may be re-written as a Boolean expression, which allows the memory to behave as combinatorial logic, however, the more regular the pattern, the more the expression can be simplified.

The requirements of a pattern to be preloaded in memory are:

a) we can observe a '1' or '0' on any of the read address inputs;

b) we can set a '1' or '0' on any of the read data outputs;

Preferably the pattern is also chosen so that:

c) the pattern can be represented by a simple logic function;

d) the pattern data can easily be generated from the address bit pattern;

The simplest pattern for a RAM is data = address, the pattern being replicated as many times as necessary to fill all the bit positions in the data word. An example pattern is shown in Figure 8. In this case, the data generator in the preloader is simply wires or other electrical connections so that the data equals the address.

The data generator to create this pattern is shown in Figure 9. As can be seen, by selecting such a simple pattern, the data generator is simply a connection from each address bit to a corresponding data bit. The corresponding logic model of the RAM is shown in Figure 10, and is the same as the data generator except for the addition of buffers 82 at the appropriate locations. This is to ensure that every input and output is independent.

In one embodiment, the pattern generator is comprised of an enabled address counter. The pattern is simply a logical function of the address.

<u>For an 8X16 RAM (or RAM/CAM):</u>

RA	Q
000	0000000000000000

001 1001001001001001

010 0010010010010010

011 1011011011011011

100 1100100100100100

101 1101101101101101

110 0110110110110110

111 1111111111111111

For 8 words, there are three address bits RA [0], RA[1], RA[2] producing 2^3=8 addresses as shown. With the pattern above, these address bits map onto the outputs Q as follows:

RA[0] maps to Q[0], Q[3], Q[6], Q[9], Q[12], Q[15]

RA[1] maps to Q[1], Q[4], Q[7], Q[10], Q[13]

RA[2] maps to Q[2], Q[5], Q[8], Q[11], Q[14]

The real input bit thus produces a deterministic output, which is consistent for each test.

For a 8X16 RAM/CAM:

C[15:0]==0000000000000000 maps to M[7:0]=00000001

C[15:0]==1001001001001001 maps to M[7:0]=00000010

C[15:0]==0010010010010010 maps to M[7:0]=00000100

C[15:0]==1011011011011011 maps to M[7:0]=00001000

C[15:0]==0100100100100000 maps to M[7:0]=00010000

C[15:0]==1101101101101101 maps to M[7:0]=00100000

C[15:0]==0110110110110110 maps to M[7:0]=01000000

C[15:0]==1111111111111111 maps to M[7:0]=10000000

C[15:0]==anything else maps to M[7:0]=00000000

For a CAM, the data = address pattern will only allow one output bit to be set high at a time. A checker board pattern is preferred instead, the logic function being represented by inverters, buffers and two multi input AND gates. One embodiment of such a data generator is shown in Figure 11 and comprises an inverter and interconnections so that a sequence of repeating 1's and 0's is presented at the memory data input. The logic function the loaded memory represents is shown on Figure 12 for an 8 x 8 CAM.

The pattern for the CAMS is the well known checkerboard and inverse checkerboard, used respectively for even and odd addresses.

For an 8X16 CAM:

0101010101010101

1010101010101010

0101010101010101

1010101010101010

0101010101010101

1010101010101010

0101010101010101

1010101010101010

This means that:

C[15:0] == 0101010101010101 maps to M[7:0]=01010101

C[15:0] == 1010101010101010 maps to M[7:0]=10101010

C[15:0] == anything else maps to M7:0]=00000000

The problem addressed by the embodiment was that generally GBUsoftrams are too small and numerous to use Built in Self Test (BIST) technology, but that during combinational ATPG, the GBU RAMS are treated as "black boxes" (or X generators because ATPG tools don't know how to deal with memories in combinational mode) which

means that fault coverage is lost by propagating unknown values. That is, Logic in the RAM's control path is unobservable, and logic in the observe path is uncontrollable, the write logic, is observable because the write port is scanned.

As described, the wrapper initializes the memory contents with a known pattern on each memory location, which will make the RAM deterministic and rendered in the ATPG model as a collection of combinational gates and not a memory model.

The overall view of testing with a preloaded memory is shown in Figure 12. Namely, an example of an entire system using the present invention is provided. Logic 10 in the input write path is shown, after which is positioned the wrapper 40. According to the invention the wrapper 40 connects to and interacts with the memory core 30 in the manner explained. Additional logic 10 may exist in the read address path and also in the read data path as shown.

This improves fault coverage during combinational ATPG, uses a low silicon area, is a simpler ATPG Model. Also, the wrapper circuit uses flip flops which are scanable.

Using the wrapper to write in the memory exercises the read and write decode logic. Therefore the algorithm applies during pattern mapping (macrotest) can be simplified from 6N to 4N. This brings a significant decrease in the number of Macrotest/Pattern Mapping vectors. This results in test time reduction especially if the number of flip-flops per scan chain is high.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.